IN THE CLAIMS:

Please cancel claims 1-13 and 21-26.

1.-13. (canceled)

14. (Previously Presented) An antifuse, comprising:

a first conductive region, the first conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge;

a nonconductive region adjoining the first conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are In facing relationship and form an interface;

a dielectric layer disposed over at least a portion of the first upper surface of the first conductive region, at least a portion of the edge, and at least a portion of the second upper surface, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer; and

a second conductive region on the dielectric layer.

15. (Original) The antifuse of claim 14, wherein the first conductive region defines a corner and wherein the dielectric layer is disposed over the corner.

16. (Original) The antifuse of claim 14, wherein the first conductive region and the nonconductive region form a substantially planar upper surface which interfaces with a lower surface of the dielectric layer.

17. (Original) The antifuse of claim 14, wherein the dielectric layer is disposed over at least a portion of the nonconductive region.

18. (Original) The antifuse of claim 14, wherein the nonconductive region comprises at least one of SiO_2 and SiN.

19. (Original) The antifuse of claim 14, wherein the dielectric layer comprises SiN.

20. (Original) The antifuse of claim 14, wherein the nonconductive region comprises at least one of SiO_2 and SiN and wherein the dielectric layer comprises SiN.

21.-26. (Canceled)

Please add the following claims:

27. (New) The antifuse of claim 14, wherein the first conductive region and the nonconductive region are formed in a substrate for forming the antifuse.

28. (New) A method for producing an antifuse structure, comprising:

forming a conductive region, the conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge;

forming a nonconductive region adjoining the conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface; and

forming a dielectric layer over at least a portion of the first upper surface of the conductive region, at least a portion of the edge, and at least a portion of the second upper surface, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer.

29. (New) The method of claim 28, forming a conductor on the dielectric layer.

30. (New) The method of claim 28, wherein the conductive region defines a corner and wherein forming the dielectric layer comprises forming the dielectric layer over the corner.

31. (New) The method of claim 28, wherein the first lateral boundary surface is substantially orthogonal to a lower surface of the dielectric layer interfacing with the edge.

32. (New) The method of claim 28, wherein the conductive region and the nonconductive region are formed in a substrate for forming the antifuse structure.

33. (New) The method of claim 32, wherein the conductive region is a doped semiconductor region.

34. (New) The method of claim 32, wherein the nonconductive region comprises at least one of SiO_2 and SiN and wherein the dielectric layer comprises SiN.

35. (New) The method of claim 32, wherein the dielectric layer is disposed over at least a portion of the nonconductive region.

36. (New) A method for blowing an antifuse, comprising:

a) providing an antifuse, comprising:

a conductive region, the conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge;

a nonconductive region adjoining the conductive region, the nonconductive region, defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface; and

a dielectric layer disposed over at least a portion of the first upper surface of the conductive region, at least a portion of the edge, and at least a portion of the second upper surface; and

b) applying a programming voltage to the antifuse to form a breakdown channel in the dielectric layer, whereby an area of relatively increased field strength is produced along the edge.

37. (New) The method of claim 36, wherein the conductive region defines a corner and wherein the dielectric layer is disposed over the corner and wherein applying the programming voltage results in a further area of relatively increased field strength.

38. (New) The method of claim 36, wherein the dielectric layer is disposed over at least a portion of the nonconductive region.

39. (New) The method of claim 36, wherein the antifuse further comprises a conductor on the dielectric layer.

40. (New) The method of claim 36, wherein the conductive region and the nonconductive region are formed in a substrate for forming the antifuse.

41. (New) A method for producing an antifuse structure, comprising:

forming a first conductive region, the conductive region defining a first upper surface and lateral boundary surfaces that meet and form a corner;

forming a nonconductive region adjoining the conductive region, the nonconductive region defining a second upper surface and lateral boundary surfaces that meet at the corner of the conductive region;

forming a dielectric layer on the first and second upper surfaces overlapping at least the corner of the conductive region; and

forming a second conductive region on the dielectric layer overlapping the corner of the conductive region, whereby an area of relatively increased field strength is produced during application of a programming voltage to first and second conductive regions to form a breakdown channel in the dielectric layer proximate the corner.

42. (New) The method of claim 41, wherein the first lateral boundary surface is substantially orthogonal to a lower surface of the dielectric layer interfacing with the edge.

43. (New) The method of claim 41, wherein the first conductive region and the nonconductive region are formed in a substrate for forming the antifuse structure.

44. (New) The method of claim 43, wherein the conductive region is a doped semiconductor region.

45. (New) The method of claim 44, wherein the nonconductive region comprises at least one of SiO_2 and SiN and wherein the dielectric layer comprises SiN.